CLAIMS

1. A non-volatile semiconductor memory device comprising:

a plurality of memory cell units each including at least one memory cell formed by stacking a charge storing layer and a control gate layer above a semiconductor substrate in which data is programmed and erased by charging and discharging the charge storing layer;

a plurality of select transistors each connected to a corresponding one of the memory cell units; and

first and second transistors each for controlling a voltage to be applied to at least one of the memory cells and the select transistor connected thereto, the first transistor having a first gate insulating film, and the second transistor having a second gate insulating film with a different thickness from the first gate insulating film,

wherein a gate insulating film incorporated in the memory cell, a gate insulating film incorporated in the select transistor and the first gate insulating film are formed of substantially the same film.

2. A non-volatile semiconductor memory device comprising:

a plurality of memory cell units each including at least one memory cell formed by stacking a charge storing layer and a control gate layer above a

semiconductor substrate in which data is programmed and erased by charging and discharging the charge storing layer;

a plurality of select transistors each connected to a corresponding one of the memory cell units; and

first and second transistors each for controlling a voltage to be applied to at least one of the memory cells and the select transistor connected thereto, the first transistor having a first gate insulating film, and the second transistor having a second gate insulating film with a different thickness from the first gate insulating film,

wherein a gate insulating film incorporated in the memory cell and the first gate insulating film are formed substantially the same film, and a gate insulating film incorporated in the select transistor and the second gate insulating film are formed of substantially the same film.

3. A non-volatile semiconductor memory device comprising:

a plurality of memory cell units each including at least one memory cell formed by stacking a charge storing layer and a control gate layer above a semiconductor substrate in which data is programmed and erased by charging and discharging the charge storing layer;

a plurality of select transistors each connected

to a corresponding one of the memory cell units; and

first and second transistors each for controlling a voltage to be applied to at least one of the memory cells and the select transistor connected thereto, the first transistor having a first gate insulating film, and the second transistor having a second gate insulating film with a different thickness from the first gate insulating film,

wherein a gate insulating film incorporated in the select transistor and the second gate insulating film are formed of substantially the same film.

4. A non-volatile semiconductor memory device according to claim 1, wherein the second gate insulating film is thicker than the first insulating film.

5. A non-volatile semiconductor memory device according to claim 2, wherein the second gate insulating film is thicker than the first insulating film.

6. A non-volatile semiconductor memory device according to claim 3, wherein the second gate insulating film is thicker than the first insulating film.

7. A non-volatile semiconductor memory device according to claim 3, wherein the second gate insulating film is thinner than the first insulating film.

8. A non-volatile semiconductor memory device comprising:

a memory cell having a self-aligned double-layer gate structure which includes a gate insulating film, a first conductor serving as a floating gate layer, a second conductor serving as a control gate layer, and an insulating film electrically insulating the first and second conductors, the gate insulating film, the first conductor, the second conductor and the insulating film being formed above a semiconductor substrate; and

a transistor having a gate electrode which is formed above the semiconductor substrate and has a structure wherein a third conductor differing from the second conductor is stacked on the first conductor.

9. A non-volatile semiconductor memory device according to claim 8, wherein the gate insulating film of the memory cell and a gate insulating film incorporated in the transistor are formed of substantially the same film.

10. A non-volatile semiconductor memory device according to claim 8, wherein the third conductor has a resistance lower than the first conductor.

11. A non-volatile semiconductor memory device according to claim 8, wherein the first conductor included in the gate electrode has a conductivity type identical to that of source and drain regions

incorporated in the transistor, and the transistor has a salicide structure.

12. A non-volatile semiconductor memory device according to claim 8, wherein the third conductor is a metal.

13. A non-volatile semiconductor memory device according to claim 8, wherein the first conductor is one selected from the group consisting of monocrystalline silicon, polysilicon and amorphous silicon.

14. A non-volatile semiconductor memory device according to claim 8, further comprising a resistive element with the double-layer gate structure, the resistive element including the first conductor used as a resistor, the second conductor and the insulating film having portions thereof removed from a region of the first conductor, and the third conductor provided on the region of the first conductor.

15. A non-volatile semiconductor memory device according to claim 14, wherein the region of the first conductor on which the third conductor is formed serves as a contact region in the resistive element.

16. A non-volatile semiconductor memory device according to claim 8, further comprising an element isolating region adjacent to the transistor, and a pattern with the double-layer gate structure provided on the element isolating region.

17. A method of manufacturing a non-volatile semiconductor memory device, comprising the steps of:

forming, on a first region of a semiconductor substrate, a self-aligned double-layer gate structure which includes a gate insulating film, a first conductor serving as a floating gate layer, a second conductor serving as a control gate layer, and an insulating film electrically insulating the first and second conductors,

patterning the first conductor into a gate electrode of a transistor above a second region of the semiconductor substrate; and

providing a third conductor on the first conductor patterned in the form of the gate electrode above the second region.

18. A method of manufacturing a non-volatile semiconductor memory device, comprising the steps of:

sequentially forming, on a semiconductor substrate, a gate insulating film, a first conductor serving as a floating gate layer, an insulating film, and a second conductor serving as a control gate layer;

patterning the second conductor, the insulating film and the first conductor in a self-aligned manner in a first region of the semiconductor substrate, using a single mask, thereby forming a double-layer gate structure, and removing that portion of the second conductor which is provided on a second region of the

semiconductor substrate during the patterning of the second conductor in the first region;

forming a third conductor on the first conductor in the second region after the patterning of the first conductor in the first region, such that the first and third conductors are electrically connected to each other; and

patterning the third and first conductors into a gate electrode of a transistor in the second region.

19. A method of manufacturing a non-volatile semiconductor memory device, according to claim 17, further comprising the steps of forming an element isolating region adjacent to the transistor, and forming the double-layer gate structure on the element isolating region.

20. A method of manufacturing a non-volatile semiconductor memory device, according to claim 18, further comprising the steps of forming an element isolating region adjacent to the transistor, and forming the double-layer gate structure on the element isolating region.